

# SN54LS78A, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

SDLS200

DECEMBER 1983—REVISED MARCH 1988

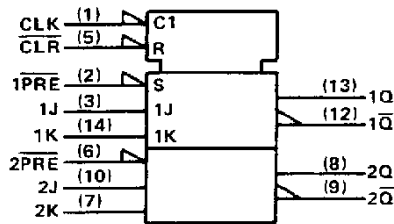
- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instrument Quality and Reliability

### description

The 'LS78A contains two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and k inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active-low inputs. When low they override the clock and data inputs forcing the outputs to the steady-state levels as shown in the function table.

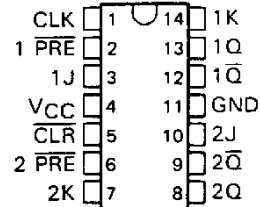
The SN54LS78A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS78A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LS78A . . . J OR W PACKAGE  
SN74LS78A . . . D OR N PACKAGE  
(TOP VIEW)



### FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>‡</sup>	H <sup>‡</sup>
H	H	↓	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

‡ This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

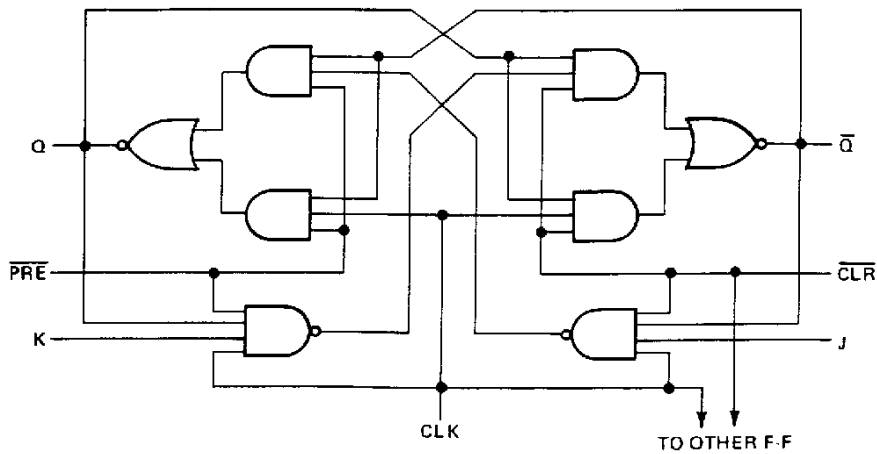
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS**  
**INSTRUMENTS**

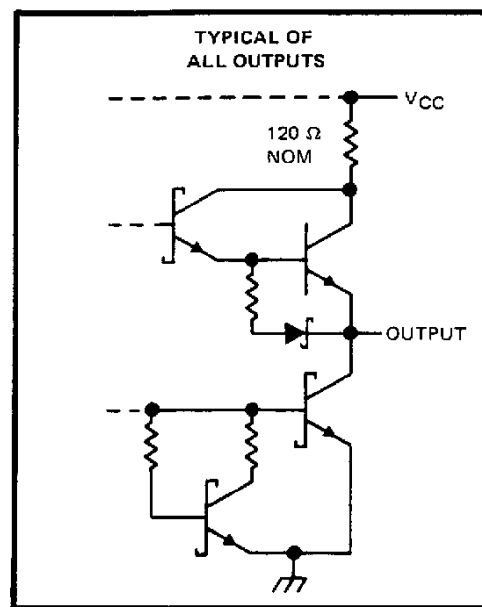
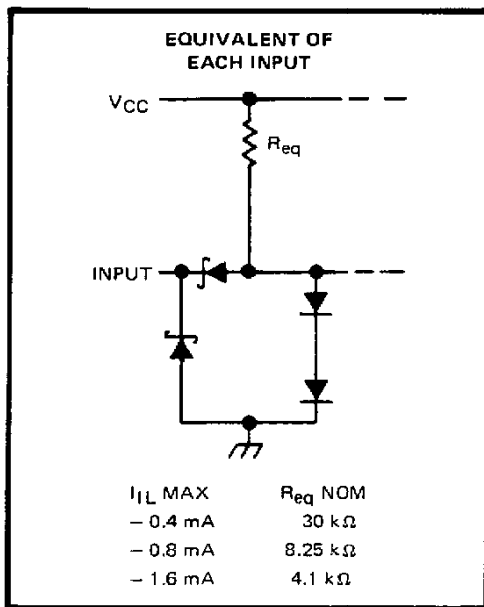
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# SN54LS78A, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

logic diagram (positive logic)



schematics of inputs and outputs (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS78A	-55°C to 125°C
SN74LS78A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# SN54LS78A, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

## recommended operating conditions

		SN54LS78A			SN74LS78A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.75	V	
V <sub>IH</sub>	High-level input voltage	2			2			V	
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V	
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA	
I <sub>OL</sub>	Low-level output current			4			8	mA	
f <sub>clock</sub>	Clock frequency	0		30	0		30	MHz	
t <sub>w</sub>	Pulse duration	CLK high		20	20			ns	
		PRE or CLR low		25	25				
t <sub>su</sub>	Setup time before CLK ↓	data high or low		20	20			ns	
		PRE or CLR inactive		20	20				
t <sub>h</sub>	Hold time-data after CLK ↓	0			0			ns	
T <sub>A</sub>	Operating free-air temperature	-55		125		0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS78A		SN74LS78A		UNIT
				MIN	TYP‡	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5	-1.5	V
V <sub>OH</sub>		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.7 V,	2.5	3.4			V
		I <sub>OH</sub> = -0.4 mA						
V <sub>OL</sub>		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V,			2.7	3.4	V
		I <sub>OH</sub> = -0.4 mA						
V <sub>OL</sub>		V <sub>CC</sub> = MIN,	V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V,	0.25	0.4	0.25	0.4	V
		I <sub>OL</sub> = 4 mA						
I <sub>I</sub>	J or K	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V			0.1	0.1	mA
	CLR					0.6	0.6	
	PRE					0.3	0.3	
	CLK					0.8	0.8	
I <sub>IH</sub>	J or K	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V			20	20	μA
	CLR					120	120	
	PRE					60	60	
	CLK					160	160	
I <sub>IL</sub>	J or K	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V			-0.4	-0.4	mA
	CLR					-1.6	-1.6	
	PRE					-0.8	-0.8	
	CLK					-1.6	-1.6	
I <sub>OS</sub> §		V <sub>CC</sub> = MAX,	See Note 4	-20	-100	-20	-100	mA
I <sub>CC</sub> (Total)		V <sub>CC</sub> = MAX,	See Note 2	4	6	4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.



**SN54LS78A, SN74LS78A**  
**DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$			$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$	30	45		MHz
$t_{PLH}$	$\overline{\text{PRE}}$ , $\overline{\text{CLR}}$ or CLK	Q or $\overline{\text{Q}}$		15	20		ns
$t_{PHL}$				15	20		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.